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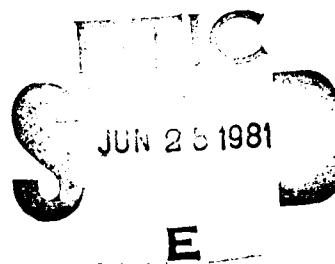
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## AUTOMATED TESTING OF MICROPROCESSOR CHARACTERISTICS IN RADIATION ENVIRONMENTS

Spire Corporation

Frederic L. Milder



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APPROVED:

*Walter M Shedd*

WALTER M. SHEDD  
Project Engineer

APPROVED:

*Clarence D. Turner*

CLARENCE D. TURNER  
Acting Director, Solid State Sciences Division

FOR THE COMMANDER:

*John P. Huss*

JOHN P. HUSS  
Acting Chief, Plans Office

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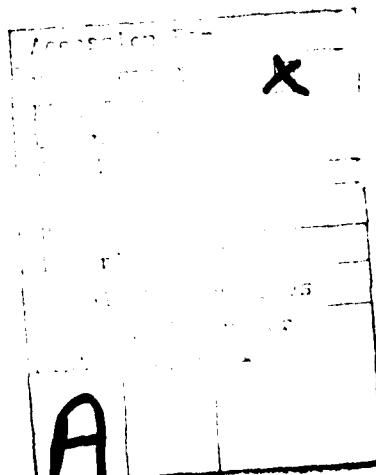
development for running test system with TMS 9900.

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## EVALUATION

This is the final report under contract F19628-78-C-0118. The objective of this program was the development of efficient methods for the automated testing of microprocessors and other LSI circuits in radiation environments. The program has resulted in a test system capable of detecting both transient and permanent failures caused by radiation and also capable of recording the errors all under the control of a reference microprocessor. The system compares the results of the device under test with a reference device and thus is adaptable to a variety of circuits. The report covers the period from May 1978 - June 1980 and summarizes the design of the test system which is expandable up to 64 test lines. This effort was part of the radiation hardened technology program under TPO R&D.

*Walter M. Shedd*

WALTER M. SHEDD  
Project Engineer

## SECTION 1

### INTRODUCTION

This is the final report for contract number F19628-78-C-0118 (contract dates 30 May 1978 - 30 June 1980). The objective of this program as stated in the contract was to "perform an investigation to identify and develop efficient methods for the automated testing and characterization of radiation hardened microprocessors and integrated circuits that will be functioning as components of C<sup>3</sup>". In this regard Spire has performed the following tasks:

1. Set up, interfaced and debugged a Texas Instruments 92K magnetic bubble memory unit for use with a TMS 9900/100M microcomputer;
2. Set up, tested, expanded and interfaced as necessary, major components for the development of radiation testing programs and procedures of three microprocessors which were of interest: RCA 1802, TI 9900 and Motorola 6800;
3. Developed test procedures based on limited, reasonable coverage in a specific logical sequence designed to test microprocessors for failure modes (after radiation damage) and identify the problem areas in the hardware.
4. Designed, built and partially debugged a microprocessor test unit which is capable of detecting and recording both transient and "permanent" upset errors in operating processors during either pulsed or continuous radiation exposure (8 channels currently, expandable to 64).
5. Designed and built the necessary interface hardware and developed the necessary software codes to enable a test of the TMS 9900 microprocessor on the above system.

Section 2 of this report covers the concepts developed in the course of the contract and explains how they contribute to the overall picture of the radiation testing of microprocessors and other LSI circuits. Section 3 summarizes the work performed during the first year of the contract. Section 4 reviews the past year. Finally, Section 5, contains recommendations for the directions of future work.

## SECTION 2 TESTING CONCEPTS

The approach taken to the radiation hardness testing of microprocessors and LSI circuits was three pronged (see Figure 1). At the most basic level, to test any LSI circuit properly, no matter what the procedures, a familiarity with that circuit must be developed. This was most easily done through working with the circuits in question. Thus, one aspect of the contract was centered around setting up, interfacing, evaluating, expanding and becoming generally familiar with the following components:

- RCA COSMAC development/evaluation system
- RCA CDP 1802 based microcomputer
- Tektronix 4024 display terminal
- RCA floppy disk memory
- Texas Instruments TMS 9900/100M microcomputer
- Texas Instruments TMS 990/302 development system
- Motorola 6800 based microcomputer
- Tektronix S-3260 LSI test system
- Texas Instruments 92K bubble memory (BKA 0203A)

The second prong of the approach was to develop the concept for testing procedures capable of finding faults in the hardware of functioning microprocessors induced by radiation damage. These procedures were to use the Tektronix S-3260 system as the testing apparatus. The concept developed was to examine the processor, one functioning area at a time, e.g. data bus buffer and data bus, then the data register, then the scratch and register, etc. Thus, for example, in checking the data register, one would be assured that any error was indeed from that register and not from the bus. In this concept one would basically "walk through" the processor from the outside in, that is, from the most I/O oriented hardware to the most internal registers and data paths. After identifying this technique as desirable, a program flow chart to partially test the RCA CDP 1802 microprocessor was developed to demonstrate the concept. The above work, except for that dealing with the TMS 9900/100M and the TMS 990/302, was performed during the first year of the contract. The second year was spent on the concepts and work described below.

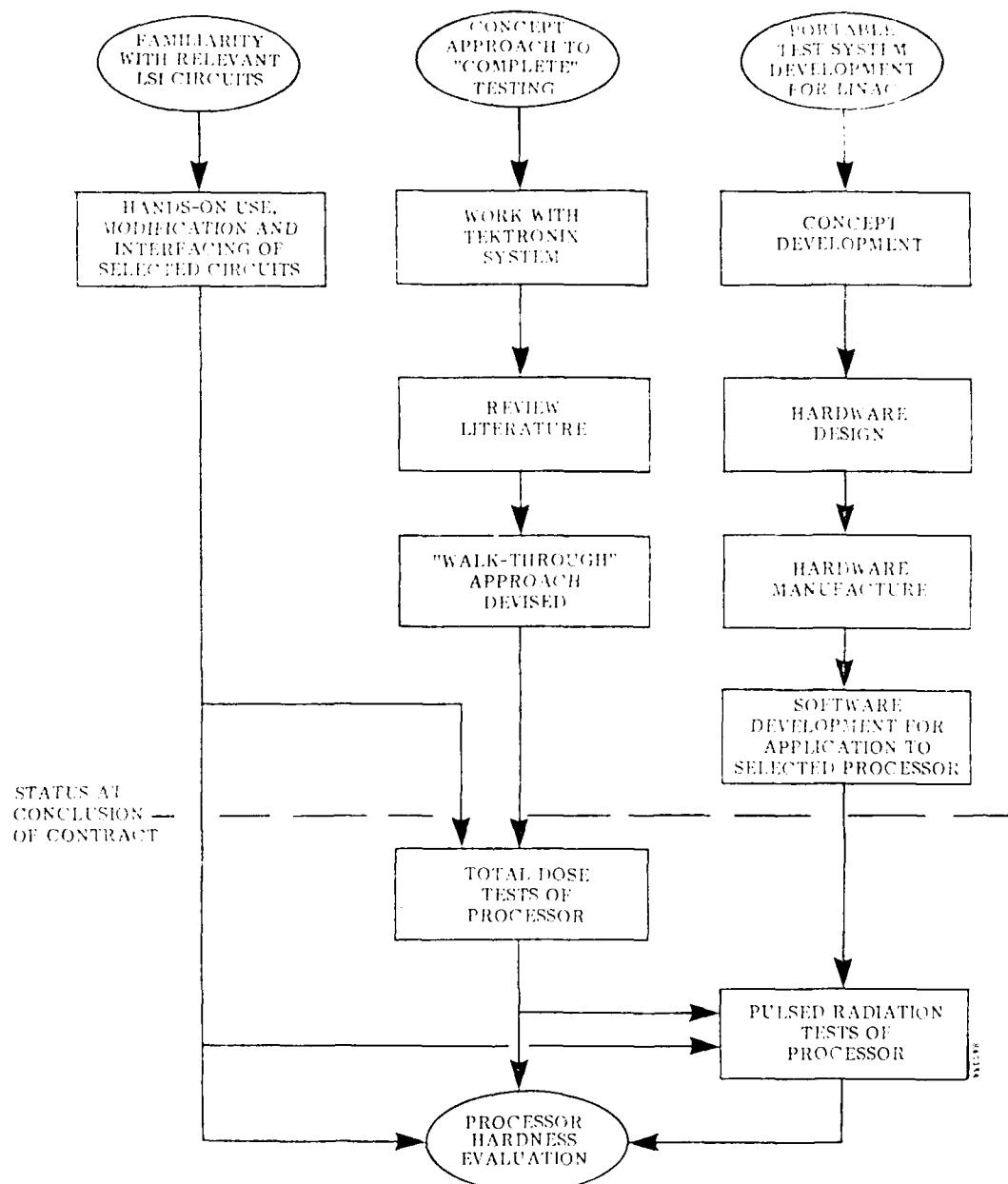


FIGURE 1. THREE-PRONGED APPROACH TO RADIATION TESTING OF MICROPROCESSORS

Since the S-3260 system is rather large and immobile, the above test procedure only has utility for permanent damage detection. That is, it is valuable for total dose failure tests wherein the device can be tested, exposed to radiation of a given quantity and then tested again. It is not useful for transient error detection or bit errors which do not involve permanent latchup, etc. Neither is it suited for testing for failures during pulsed radiation exposure, since at present it has no hookup to the LINAC test area. For this reason a third prong to the total testing approach was necessary.

To test a microprocessor in the pulsed environment at the LINAC, a portable hardware system capable of detecting and recording errors had to be developed. The design used is based on comparing a device under test (DUT) to a reference device (RD), pin for pin. Since the RD had to be a microprocessor itself, and since such a test system would naturally be run by some sort of smart logic, it was decided to use the RD as the controlling device as well. Thus, a comparator system was built, one which could compare 8 pin pairs (expandable up to 64) and detect logic errors, transient errors, and parametric failures. However, the comparator system itself is not smart. Rather, the RD is incorporated into a microcomputer which controls the comparator system and provides the test sequence for the DUT as well. This concept is depicted in Figure 2. Included in this design is a good degree of flexibility in the comparator system. Thus, for each microprocessor type to be tested, the comparator system hardware is modified slightly (mostly cabling), and a new RD/microcomputer and DUT are integrated into the system. The comparator system, as described, was designed and built, and a TMS 9900 RD and DUT were chosen for the first testing. Debugging of the entire integrated system has not been completed to this date.

$\mu P_{RD}$ : REFERENCE MICROPROCESSOR AND SYSTEM CONTROLLER  
 $\mu P_{DUT}$ : MICROPROCESSOR UNDER RADIATION TESTING  
 MICROCOMPUTER BOARD

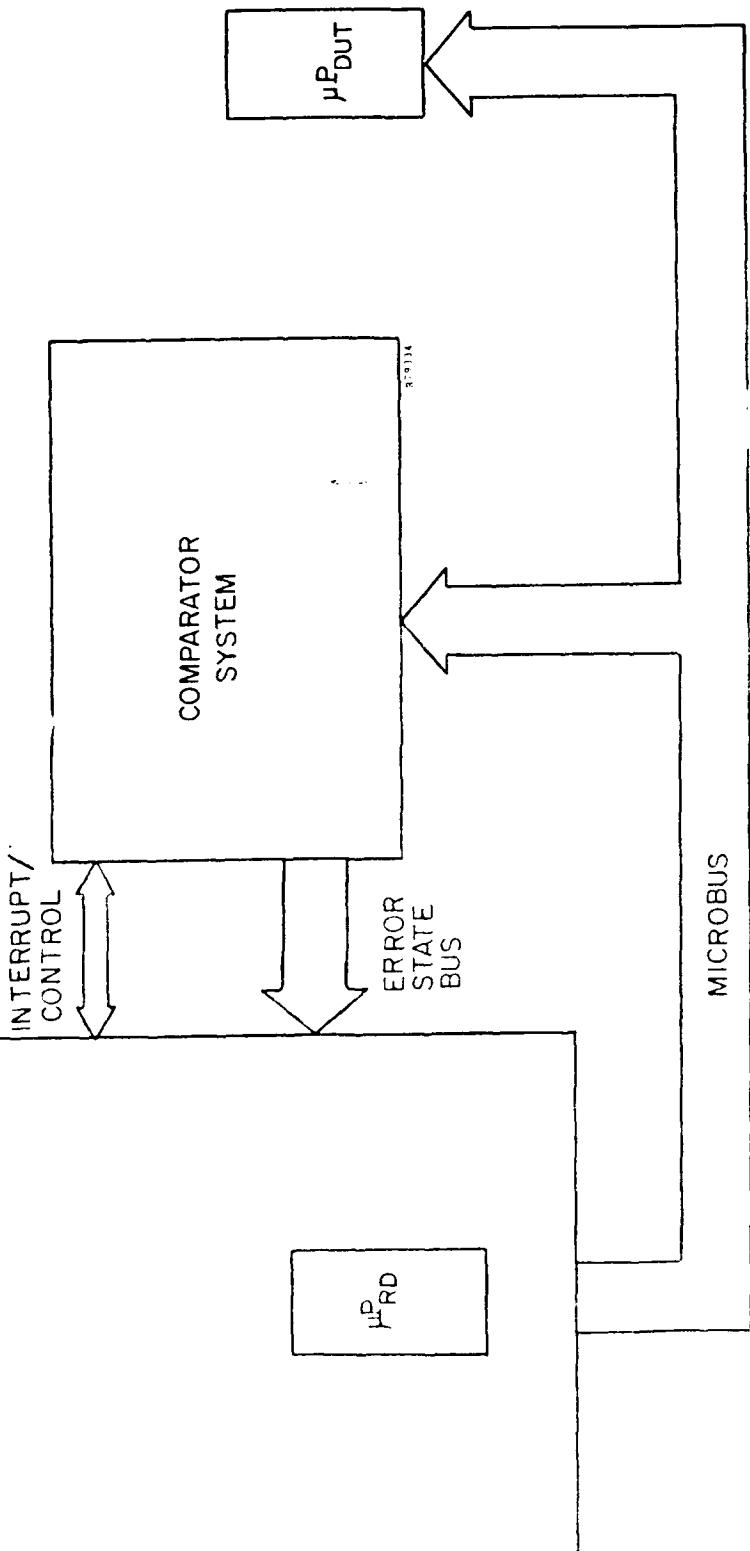


FIGURE 1. MICROPROCESSOR TEST SYSTEM CONCEPT USING REFERENCE DEVICE AS CONTROLLER

### SECTION 3

#### REVIEW OF FIRST YEAR OF CONTRACT

As previously stated, the first year of the contract was spent in two endeavors. One was to gain familiarity with the detailed workings of several microprocessors, the Tektronix S-3260 system and a bubble memory through a hands-on development of the hardware and software. The details of this process need not be included here, since an insignificant amount of new knowledge was produced in this regard, although many minor problems had to be overcome in the area of component interfacing. This work is generally reviewed in more detail in AR-10059.

The second major endeavor was to define procedures to systematically test a microprocessor (RCA CDP 1802 in particular), and identify malfunctioning regions of the processor in a "comprehensive style" test (i.e., not exhaustive, but complete). The test was supposed to take a reasonable length of time on the S-3260 system. It was decided, through literature research and discussions, that it was best to use methods which rely heavily on concepts like commonality of data paths and of functions and subfunctions. For instance, if two registers of an on-chip register array can be shown to be able to be loaded (separately, via a common internal data bus) into the accumulator, and if data from one register can be shown to be properly added to the contents of the accumulator, then the proper addition of data from the second register into the accumulator need not be explicitly tested.

The subfunction approach recognizes the fact that execution of any of the instructions of the microprocessor repertoire involves sequential and parallel usage of some subset of the relatively small number of intermediate-level functional blocks or subfunctions. Typical of these functional blocks are, for example, address and data buffers, the ALU, scratch pad registers, the instruction register and decoder, the accumulator register, etc. Thorough testing of some register, for instance, by multiple, varied usage of any one instruction, and then testing all over again using another instruction, is an example of the high redundancy of the "exhaustive" approach, which can be readily eliminated.

The thorough testing of a register array brings up two further considerations concerning simplification. Ideally, a register array should be tested with all possible

(i.e.  $2^{16} = 65,536$ ) words, one register at a time (thereby ignoring possible, but hopefully very slight, interregister interactions). One simplifying assumption is that in a particular class (i.e. on-chip scratch pad) of registers, one is the same as any other as regards radiation effects and hardness. Accordingly, only one register of each class need be thoroughly tested. If different registers (or sets of registers) reside at different places on the chip, long access paths to some but not other registers may vitiate the assumption of identical registers.

A second, more extensive simplification concerns the ideal 65K-word test of one or more of the registers. Semiconductor memory manufacturers are faced with the same problem and resort to testing with various "bit patterns". Among the more than 100 such patterns developed are all one/all zeros, checkerboard, walking ones, surround/disturb, etc. A dozen or so well-chosen test words should provide fairly complete coverage. Added to the above concepts is the additional comment that the most reasonable approach in any one processor would be to start with the functional blocks which are closest to the I/O paths and to work "inward" from there.

As an example of these procedures, a partial test of the RCA CDP 1802 microprocessor which was specifically oriented toward execution on the Tektronix S-3260 automated LSI test system was flow charted. It is in the form of a "dialog" between the microprocessor and the LSI tester, typically in the form:

1. Microprocessor requests next instruction
2. S-3260 checks levels and supplies the next instruction
3. Microprocessor inputs this "fetched" instruction, decodes it and executes it
4. S-3260 supplies requisite "memory requests" and tests resulting output levels.

Preparation for generating this testing procedure involved analysis of available technical literature on the 1802 internal architecture — to establish data paths, major registers and functions, any temporary or "hidden" registers or "transparent buffers", etc. — as well as the explicit details of the complete instruction set, so as to determine what can be or must be determined, and in what order.

The resulting test procedure was included as Appendix I of the annual report AR-10059.

## SECTION 4

### REVIEW OF SECOND YEAR OF CONTRACT

One major effort during the second year concerned the conceptual design, detail design and fabrication of the portable, self-contained system capable of detecting and recording transient upsets in microprocessors. The system concept is to compare a device under test (DUT) to a reference device (RD) which is simultaneously controlling the test system. As the system concepts developed, the block design of the system changed from that given in Figure 2 to that shown in Figure 3. The more detailed design of Figure 3 and the design of the comparator system shown in Figure 4 contain provisions for the following characteristics: (1) parametric error detectors are included which will detect transient upsets or output level errors; (2) the reference microprocessor is used as both the reference device and the controller of the test system; (3) the system records each error as it occurs, resynchronizes the DUT and RD and proceeds with further testing; (4) all pins of the DUT are tested; (5) the test instruction sequence is contained in either ROM, RAM or both, and is thus completely flexible and not limited in length.

The main hardware hurdle was the buffering of the microprocessors in such a way that the reference microprocessor could serve both as the RD and as the system controller. This was accomplished by having a bidirectional buffer for the RD and a unidirectional buffer for the DUT. (See Figure 3.) The electrical termination of the two devices is, however, equivalent. Also, the problem of resynchronizing the microprocessors after an error occurrence without having to reenter a monitor program had to be dealt with. This was achieved in a microprocessor-independent fashion by the combined use of custom hardware and a well-defined software approach. The solutions to the above problems and details of the system will be discussed in the next subsection 4.1. Subsection 4.2 deals with the adaptation of the test system to the intended radiation testing of a TMS 9900 microprocessor through software. The test system control software developed and written (in assembly language code) for the 9900 was the second area of major effort during the last year of the contract.

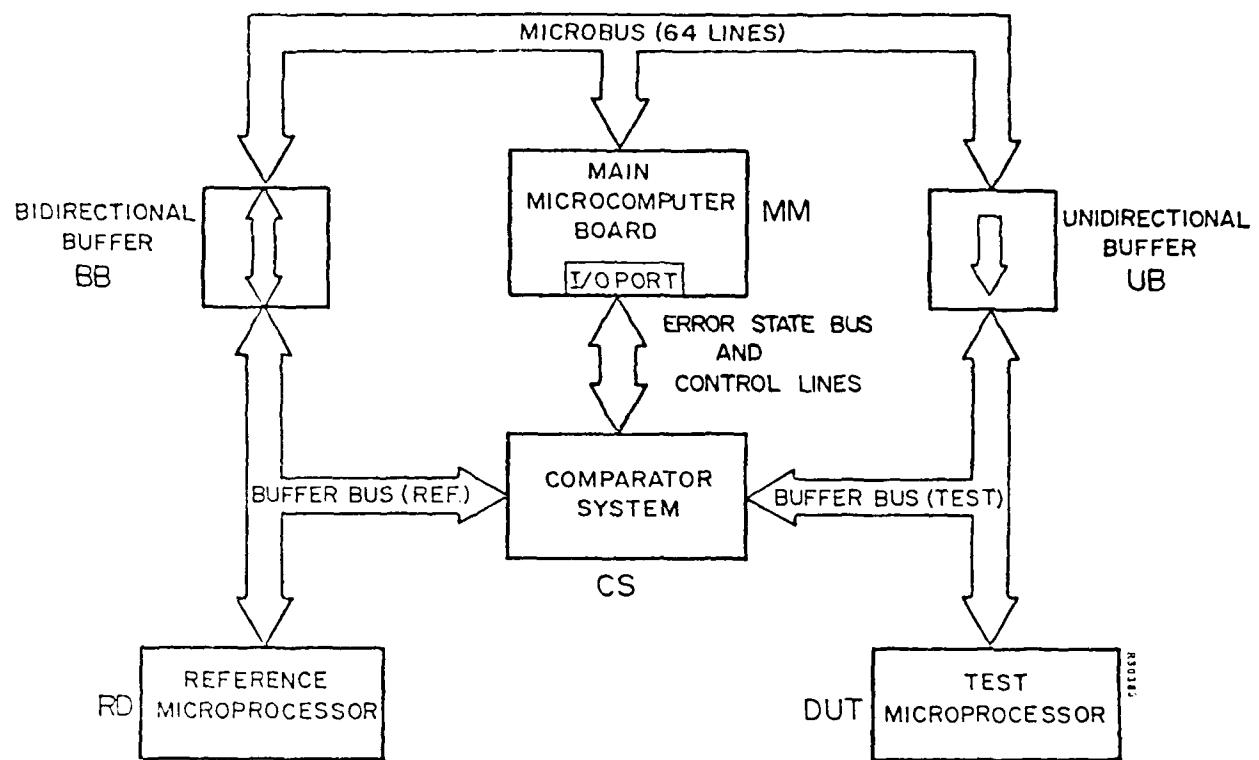


FIGURE 3. MICROPROCESSOR TEST SYSTEM BLOCK DIAGRAM

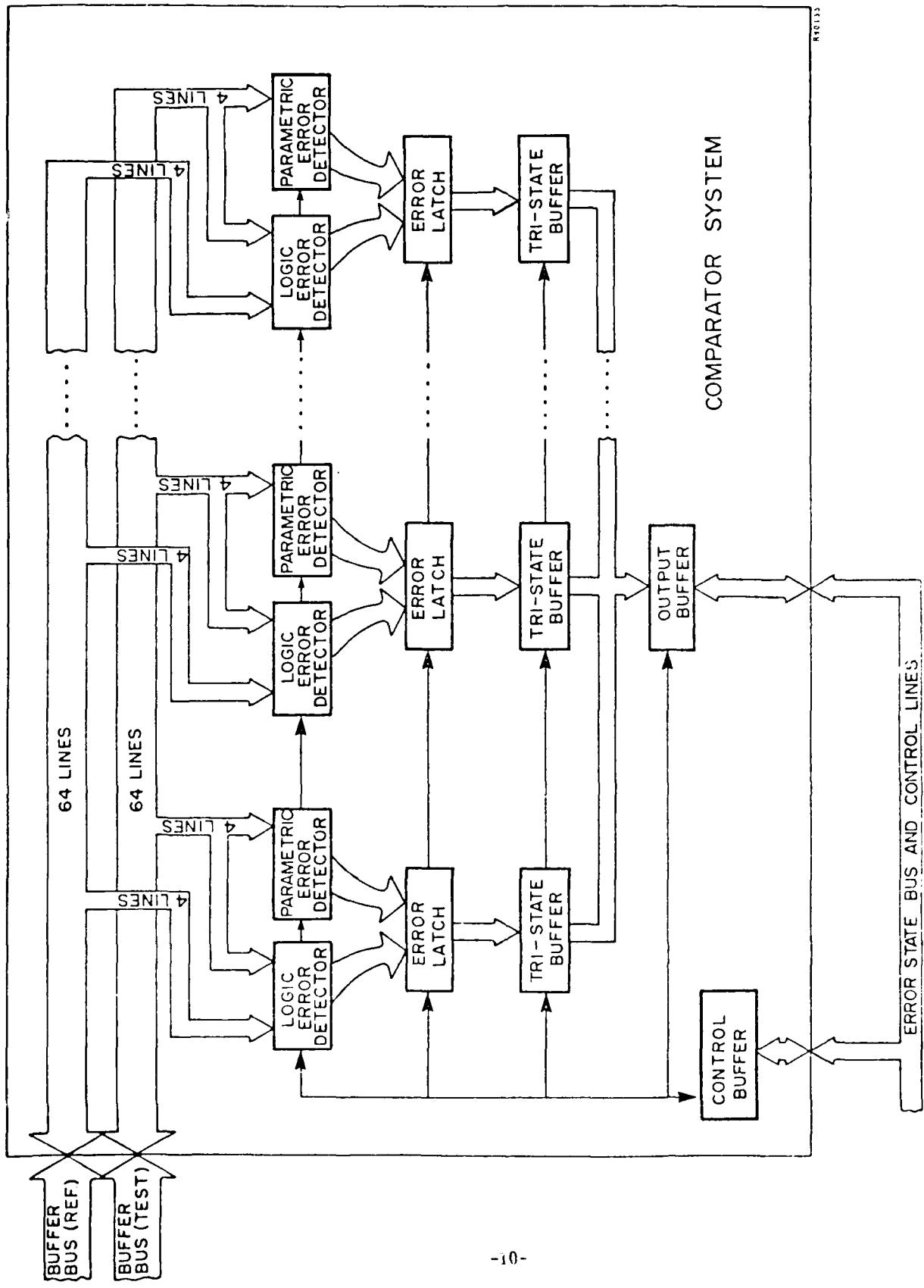


FIGURE 4. BLOCK DIAGRAM OF THE COMPARATOR SYSTEM

#### 4.1 THE MICROPROCESSOR TEST SYSTEM HARDWARE

The hardware which comprises the microprocessor test system consists of six major elements: comparator system, reference microprocessor, test microprocessor, bidirectional buffer, unidirectional buffer and main microcomputer board. Figure 5 shows this hardware, built for the system under this contract. Let us group these units into three functional groups. The first group, the RD, the bidirectional buffer (BB) and the main board (MM), make up a functioning microcomputer. Peripherals, support boards, additional memory, etc., can be added to the MM as desired in the usual fashion. The buffer is transparent to both the RD and the MM. This complete microcomputer is the controlling device for the system. The memory ROM and RAM contain (1) the monitor and monitor support codes, (2) the program codes for running the test system and (3) the actual codes designed to exercise the DUT microprocessor. The cables connecting these components are all 64 lines, so that any microcomputer on the market today can be handled. To convert the buffer from use with one microprocessor to use with another, a few control lines on the BB must be reconfigured. These lines control the breakup of the total 64 lines into input, output, power and I/O line groups, which of course change from processor to processor. The present BB is configured for a TMS 9900, since this was the major processor of interest for testing. The circuit diagram for the bidirectional buffer (Buffer Board A) and cables are included in Appendix I.

The unidirectional buffer (UB) and the DUT make up the second function group of the system. The UB is transparent for the DUT receiving input from the MM and also terminates the DUT output. Because the UB is one-way, however, the MM never receives any signals from the DUT. From the standpoint of the MM, the UB looks like a constant low. Thus, the DUT receives instructions, memory fetches, etc., from the MM in synchronization with the RD, but its outputs are ignored by the test system (except in the comparator). The UB is included in Appendix I as Buffer Board B.

The third functional group of the total system is comprised of the comparator system circuits. The block diagram was shown in Figure 4. As the DUT and the RD are functioning in parallel, the comparator system is comparing their outputs, pin for pin. The present system is built up for 8 lines only, but the design includes expansion to 64 lines. For a DUT response to be considered correct, it must pass two tests. First, it must be logically equal to the RD response. Thus, each line in the DUT is logically

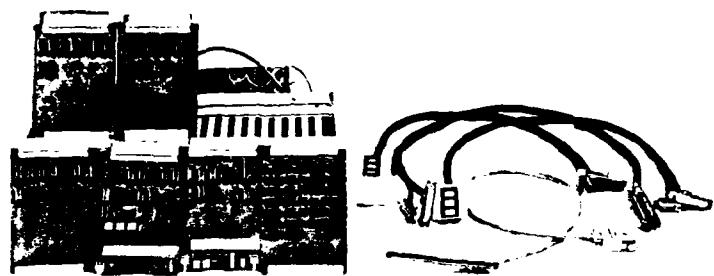
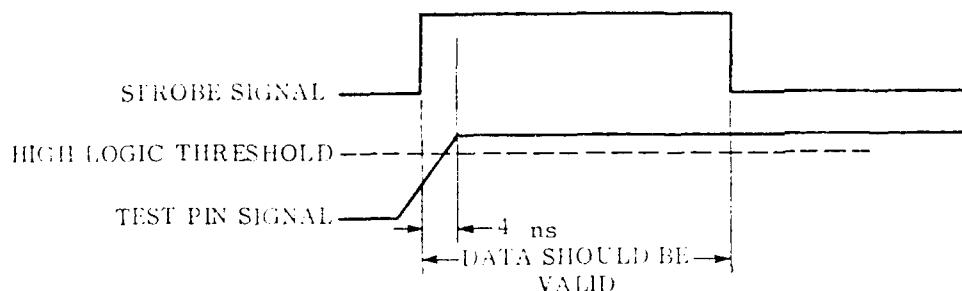


FIGURE 5. TEST SYSTEM HARDWARE: Power Supply, Card Cage  
With Backpanel Wiring, Cables, Processor Test  
Box, and Comparator, Buffer and Control Boards

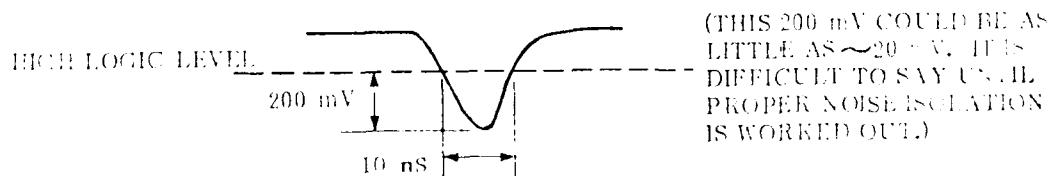
compared to the identical line in the RD. If the two are not in the same logic state for the entire time for which the data is supposed to be valid, a logic error is flagged for that line. The second test that must be passed is a parametric test. The logic level must be within certain voltage specifications for the entire data valid period for that line to pass its parametric error test. If not, a level error is declared for that line.

The possible combinations of level and logic errors which can be detected are as follows:

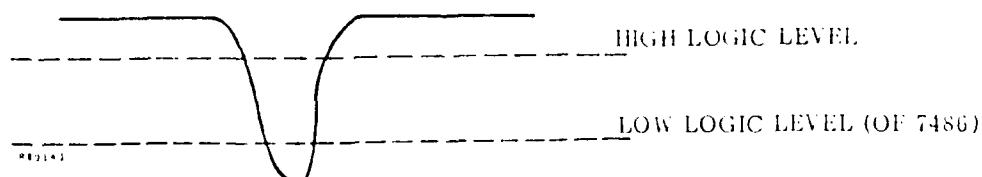
A. System will detect  $\pm 4$  ns slew on normal logic pulse; e.g., if logic high or low is not present within 4 ns of edges of strobe, system declares a level error.



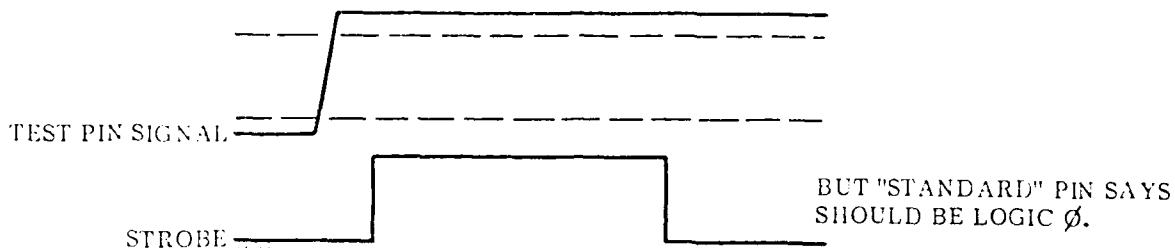
B. System will declare a level error if a "glitch" of 200 mV with 10 ns basewidth is present.



C. System declares level error and logic error if "glitch" reaches the opposite logic state.



- D. System will declare a level error for a logic signal deviating from the valid regions by >20 mV for a large fraction of the strobe width.
- E. System will declare a logic error if logic level is valid for the entire strobe width but is in disagreement with the "standard" logic state.



Once either a logic or a level error is flagged by the error detectors, that error condition and the error conditions of all the other lines being tested is latched, and a signal is sent to the control logic. The control logic then sends an interrupt to the microcomputer signalling that an error has occurred. At this point, all further signals to the comparator system are ignored, except control signals coming from the microcomputer.

The response of the computer is a set of sequential signals which turns on the tri-state buffers one at a time, along with the output buffer, so that the latched condition at the time of the error is placed on the I/O bus (for the acceptance by the computer) in one byte segments. Then the computer resynchronizes the processors (to be discussed), resets the comparator system and continues testing as desired. The entire circuits for the error detectors, latches and buffers for eight lines and the control functions are included in Appendix I as the comparator and control boards. The expansion to more pins is simply a matter of copying the detector/latch/buffer circuits as necessary and tying into the control logic (which is only a few lines).

Synchronization of the microprocessors at the initial powerup and after error detection proved to be a major difficulty. First of all, the TMS 9904 four-phase clock was not capable of driving two 9900 processors. Therefore, one 9904 was used to drive two additional 9904 clocks, one for each processor. This is shown in Figure 6. This is all right, except at powerup. After powerup, the relative phases of the two processor-driving 9904's is arbitrary. The two clocks must be brought into

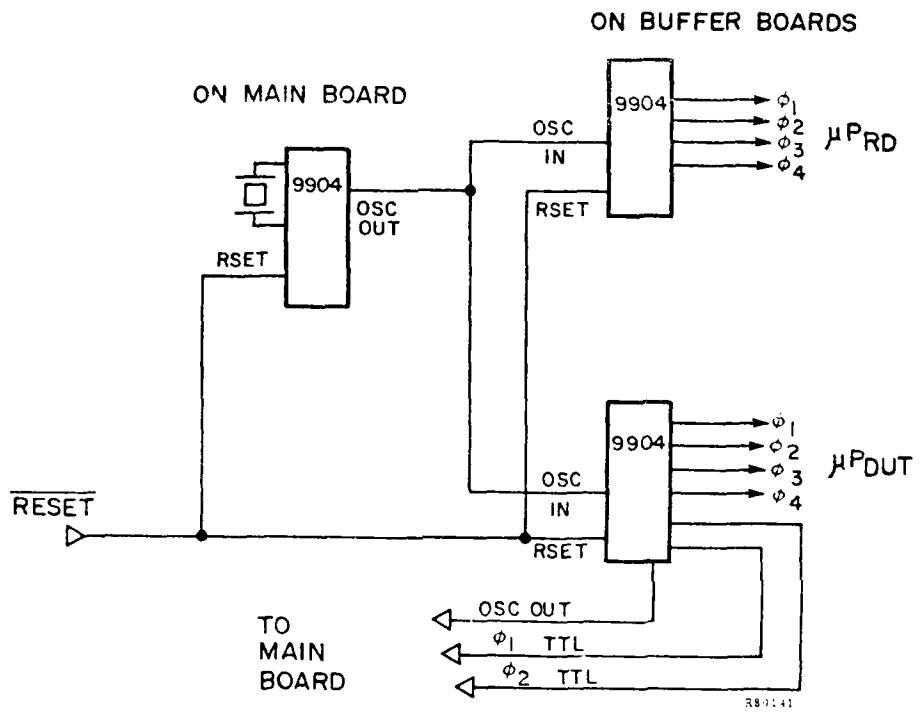


FIGURE 6. SOLUTION TO SEPARATE, SYNCHRONIZED CLOCK DRIVERS  
FOR THE RD AND THE DUT

synchronization. This problem was solved by having a gate between the primary clocks and the secondary clocks. Figure 7 shows the block diagram. The one-shots are adjusted so that every time the momentary closure is pushed, one clock pulse is removed from the OSC IN line going to one of the secondary clocks. This shifts the relative phase by 90°. The synchronization is monitored by an LED, which turns off when the clocks are in phase. The circuit for the powerup synchronization is included in Appendix I, on the buffer boards.

The second part of the synchronization problem arises when the DUT makes an error. After this occurs, the DUT is in an unknown state. In order to resynchronize the processors, a reset must be used, since on most processors a reset signal is the only one which is always responded to on the next phase-one clock pulse, no matter what the processor status. However, upon reset, one does not want to go back to a monitor; one wants to continue testing. The solution was to have the processor initiate its own reset and simultaneously set a hardware flag on the control board. It then of course responds to its reset, but before it goes to the monitor, it checks the flag. If this flag is set, it does not go to the monitor, but rather, continues testing from the point of interrupt. The circuitry for this part of the control system is also included in Appendix I, on the control board.

More discussion on the details of the subunits is included in various quarterly reports.

#### 4.2 SOFTWARE FOR THE TESTING OF THE TMS 9900

The software for the error detection, system control, error storage and test sequencing for the TMS 9900 was written during the latter part of the year, using the 990/302 development system. The code consists of four modules (SETUP, SYNC, ESCAPE, ERROR), the message list for I/O and an addition to the resident monitor called PSMON. The purposes of the modules are as follows:

SETUP - Does all of the initialization of the program: sets up workspaces, enters branch instructions into the interrupt vector locations, sets aside a stack in RAM for storage of the error conditions of the DUT and handles the proper entry or reentry into the test code. (The test code is that code, yet to be written, which will be the actual sequence of instructions that the DUT is being tested with during exposure.)

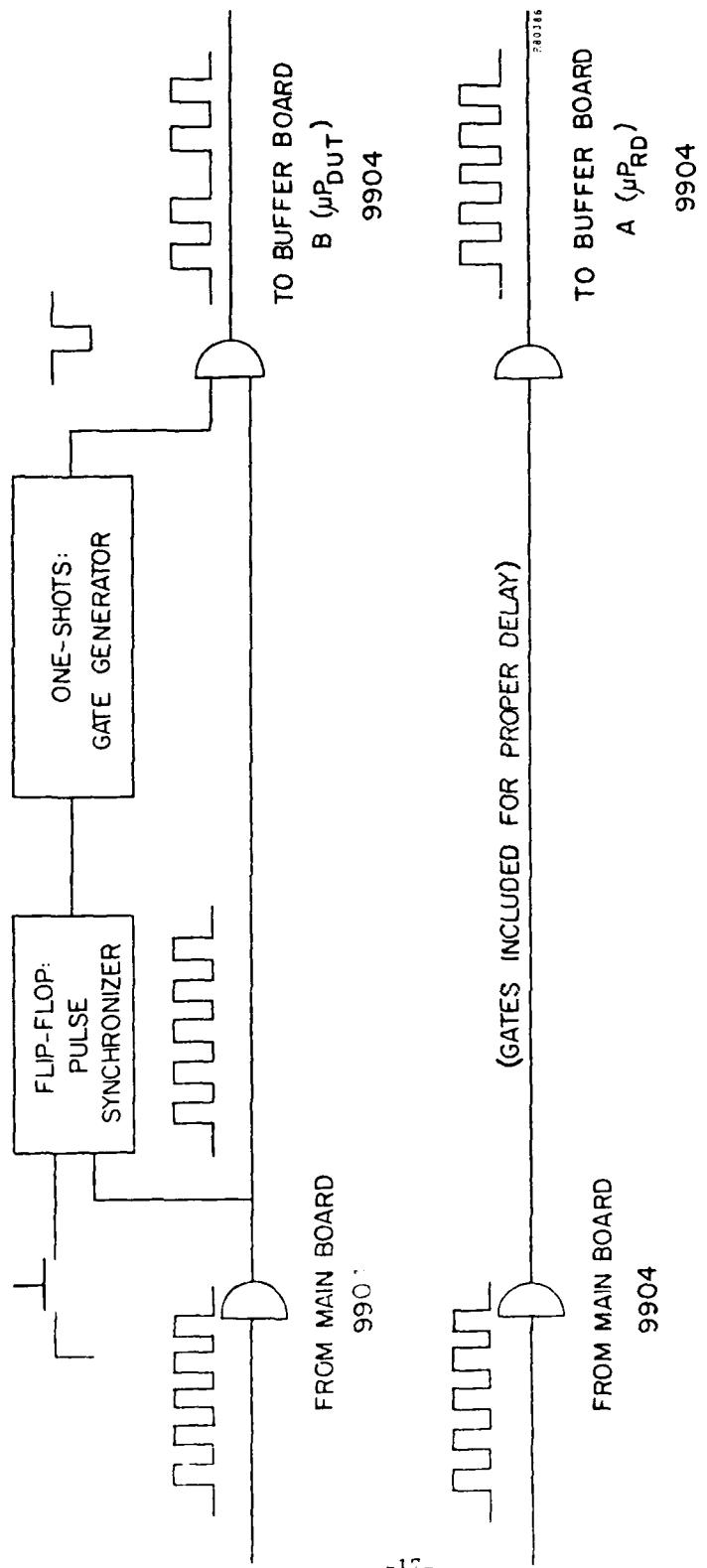


FIGURE 7. POWER-UP SYNCHRONIZATION  
 A momentary connection removes one pulse  
 from the OSC IN of the DUT 9904 clock.  
 This shifts the phase by 90°.  
 (The 9904 is a four phase clock.)

SYNC - Triggers the synchronization reset and setting of the self-reset flag.

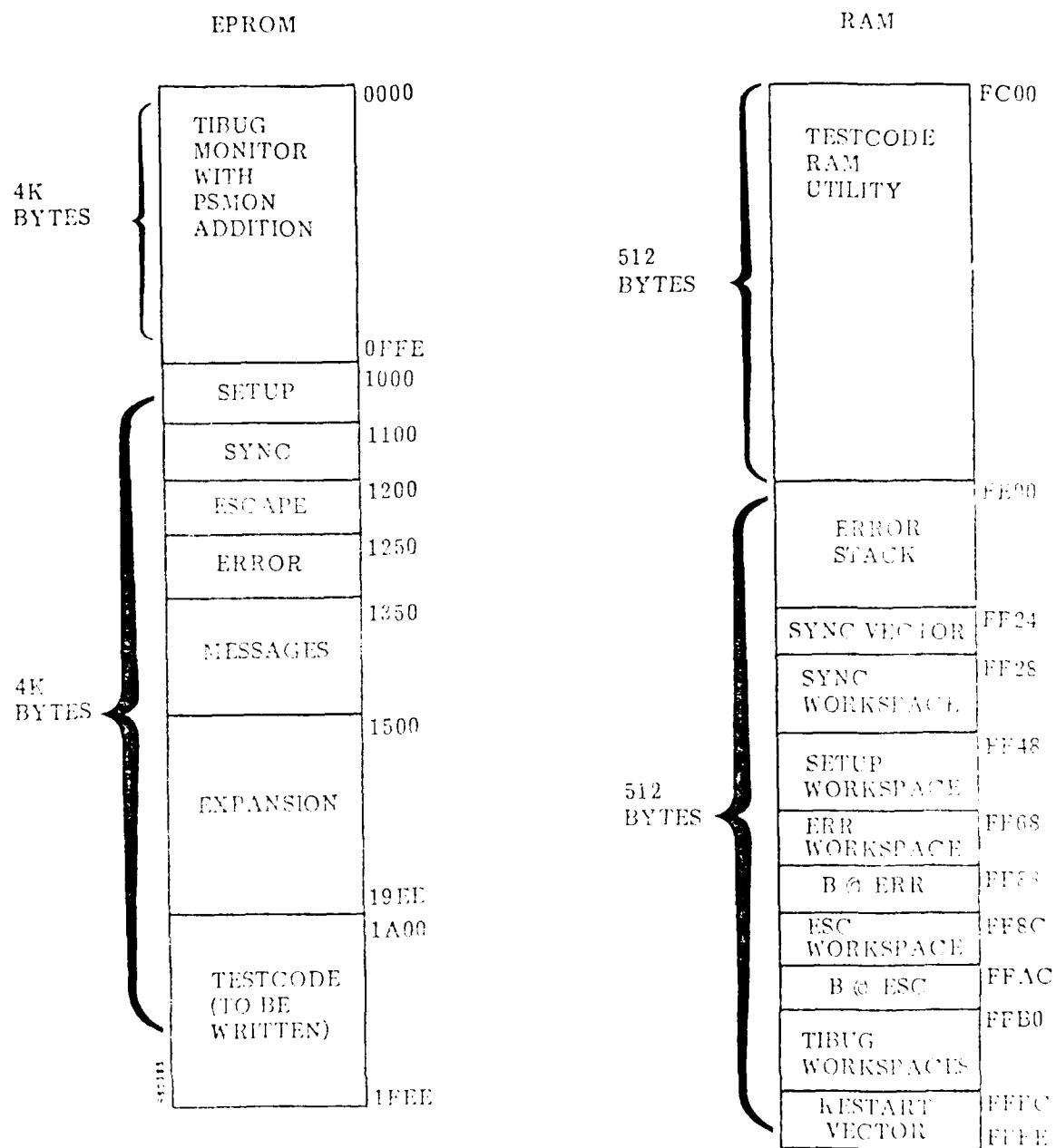
Upon return from the reset the program returns to the test code at the point of the error interrupt.

ESCAPE - Allows the escape from test code during execution: Hitting the ESC key causes a return to the monitor.

ERROR - Receives the interrupt when a DUT error occurs. It turns off the comparator system, stores the error condition one byte at a time on the error stack, tests for overrunning the allowed stack space, resynchronizes the processors through use of the SYNC module and returns.

The PSMON addition to the resident monitor precedes the first instructions normally executed by the monitor. This segment of code tests the flag which is set when the software issued reset is used. If the flag is set, the execution is transferred to the SYNC reentry point. If the flag is not set, execution is continued at the top of the usual monitor. This code addition is to be resident in the monitor EPROM (low addresses).

The memory map of the microcomputer for radiation testing is shown in Figure 8. The assembly language codes for the above modules are included as Appendix II.



## SECTION 5

### RECOMMENDATIONS FOR FUTURE WORK

#### 5.1 STATUS AT THE CONCLUSION OF THE CURRENT CONTRACT

The status of the test system hardware and software at the conclusion of the contract is as follows:

Hardware - All circuits for the testing of eight lines of a processor have been built. The adaptation of the buffer boards for the TMS 9900 has been completed, including the clock driver circuits. Cables for the 9900 board connectors have been fabricated. Board modifications of the 990/100M computer to accommodate the I/O, control and inclusion of the PSMON have been made. The monitor has been moved from 2708 EPROM's to 2716 EPROM's to allow for EPROM expansion with the relevant codes. The hardware is only partially debugged.

Software - All modules mentioned have been written and debugged. Further testing must await the complete debugging of the hardware because certain functions can only be tested with real I/O or with hardware emulation. The actual test code has not been written, and EPROM's have not been burned.

Summarizing, to bring the total system on line for testing eight lines of a TMS 9900 (four data lines, bidirectional; four address lines, output), the hardware must be debugged as a system, the software must be tested with the real hardware and the codes must be burned into EPROM.

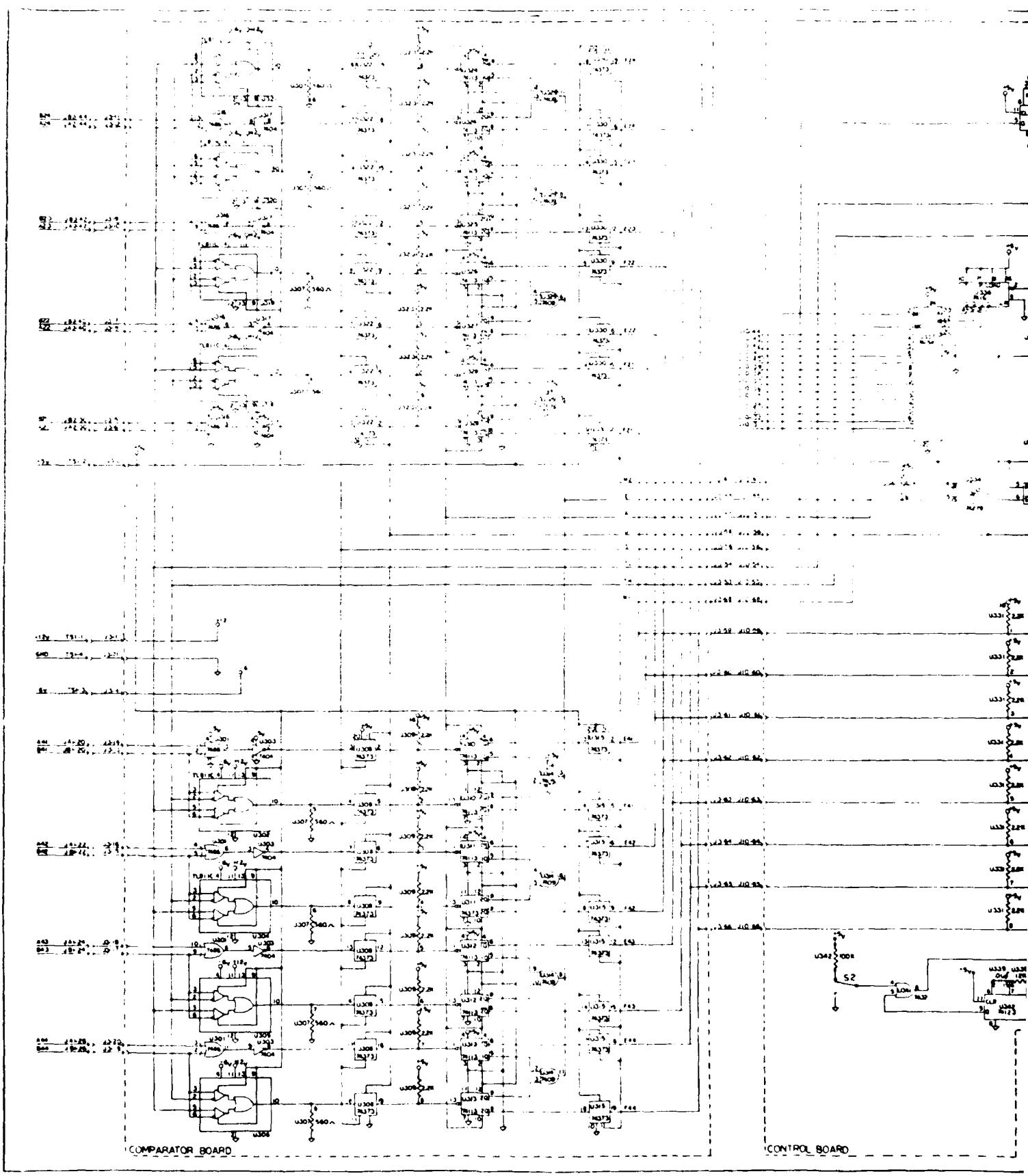
#### 5.2 FUTURE EFFORTS

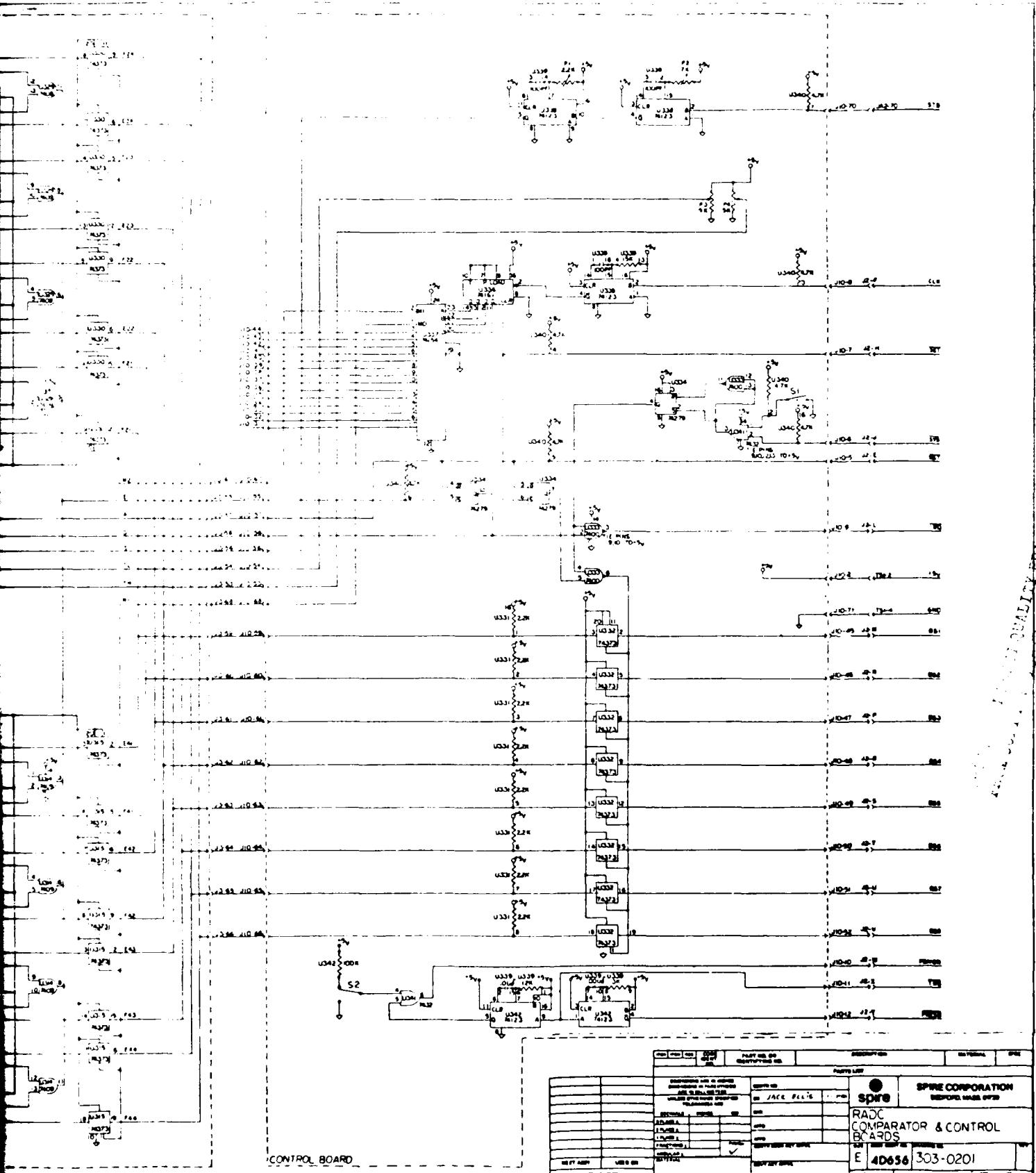
Once the system is checked out, the next major task would be the writing of the test code for the actual radiation testing. This could be approached from two possible directions. One would be to follow the concepts devised in this contract of "walking through" the processor from the outside. To do this, one would have to become more familiar with the 9900 and to go through a careful study of the internal architecture. Alternatively, one could first take a more modest approach of defining small execution

loops using only a few instructions at a time and testing these loops individually. This technique has been successfully adopted by Tom Ellis of the Naval Weapons Support Center (IEEE Trans. NS-26, 4735 (1979)). Either way, with the completion of the system developed under this contract, the combination of being able to do parametric testing as well as logic testing during pulsed radiation exposure should be a valuable and unique capability.

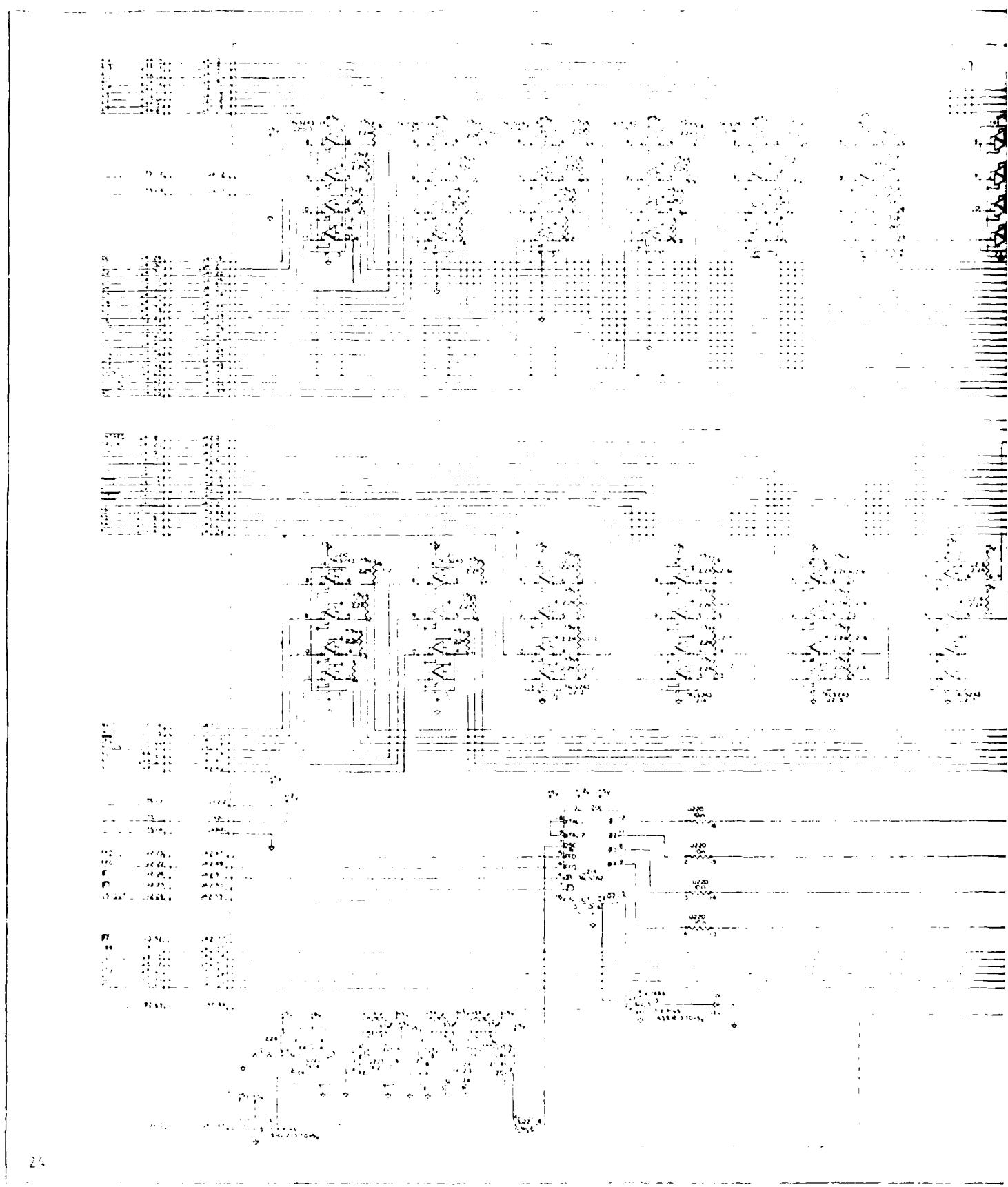
Further efforts should include work on the expansion of the system to at least 32 lines and intensive testing on the system susceptibility to interference from the LINAC. Additionally, one would want to be working on the software and hardware modifications necessary to test other processors as well as the minor modifications to the I<sup>2</sup>L version of the 9900 (SBP 9900) and, of course, to actually go ahead with radiation testing.

APPENDIX I  
CIRCUIT DIAGRAMS FOR THE  
MICROPROCESSOR TEST SYSTEM  
(Including adaptation for the TMS 9900)





## THE PRACTICABLE SCHOOL



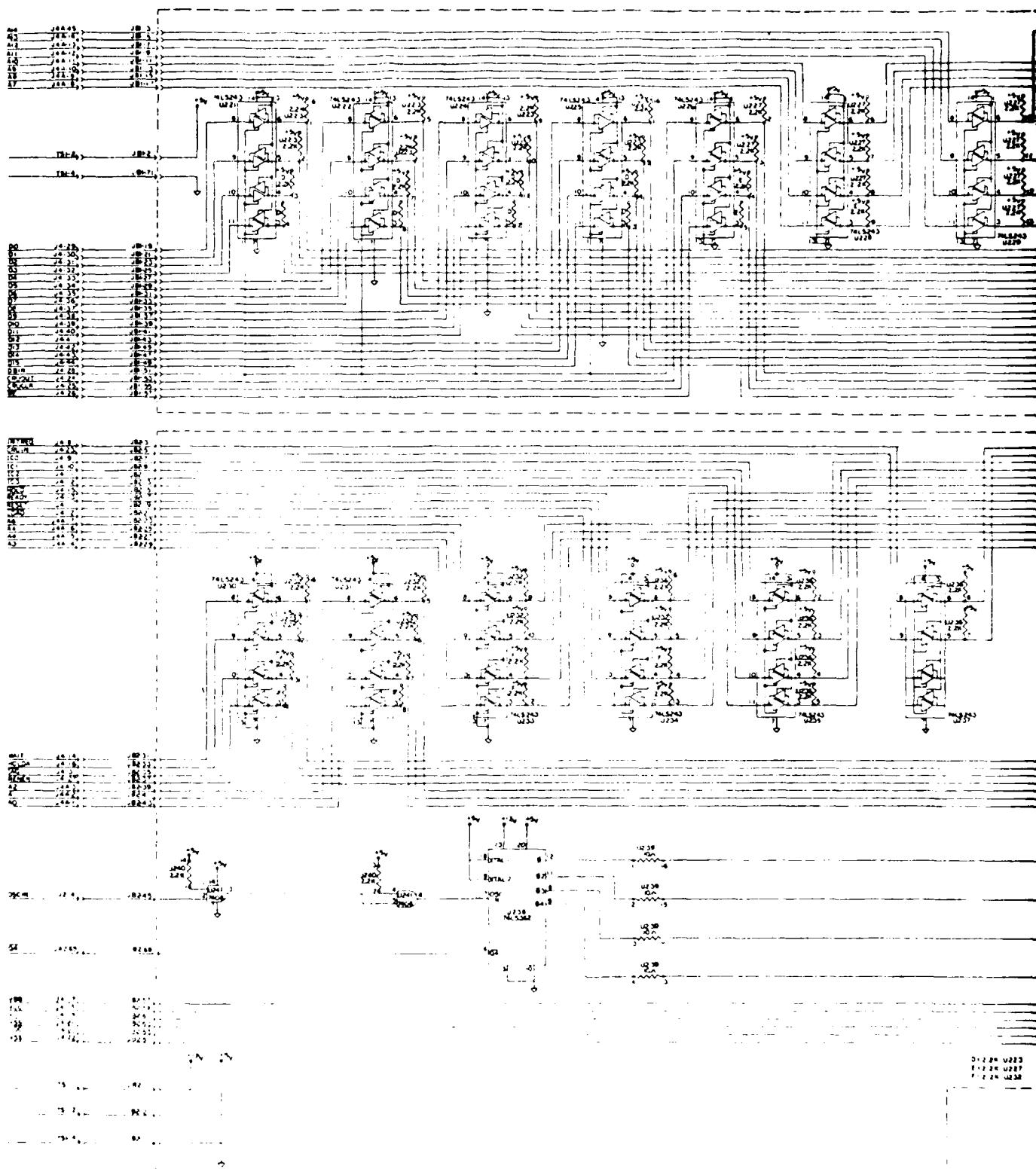
BUFFER BOARD A

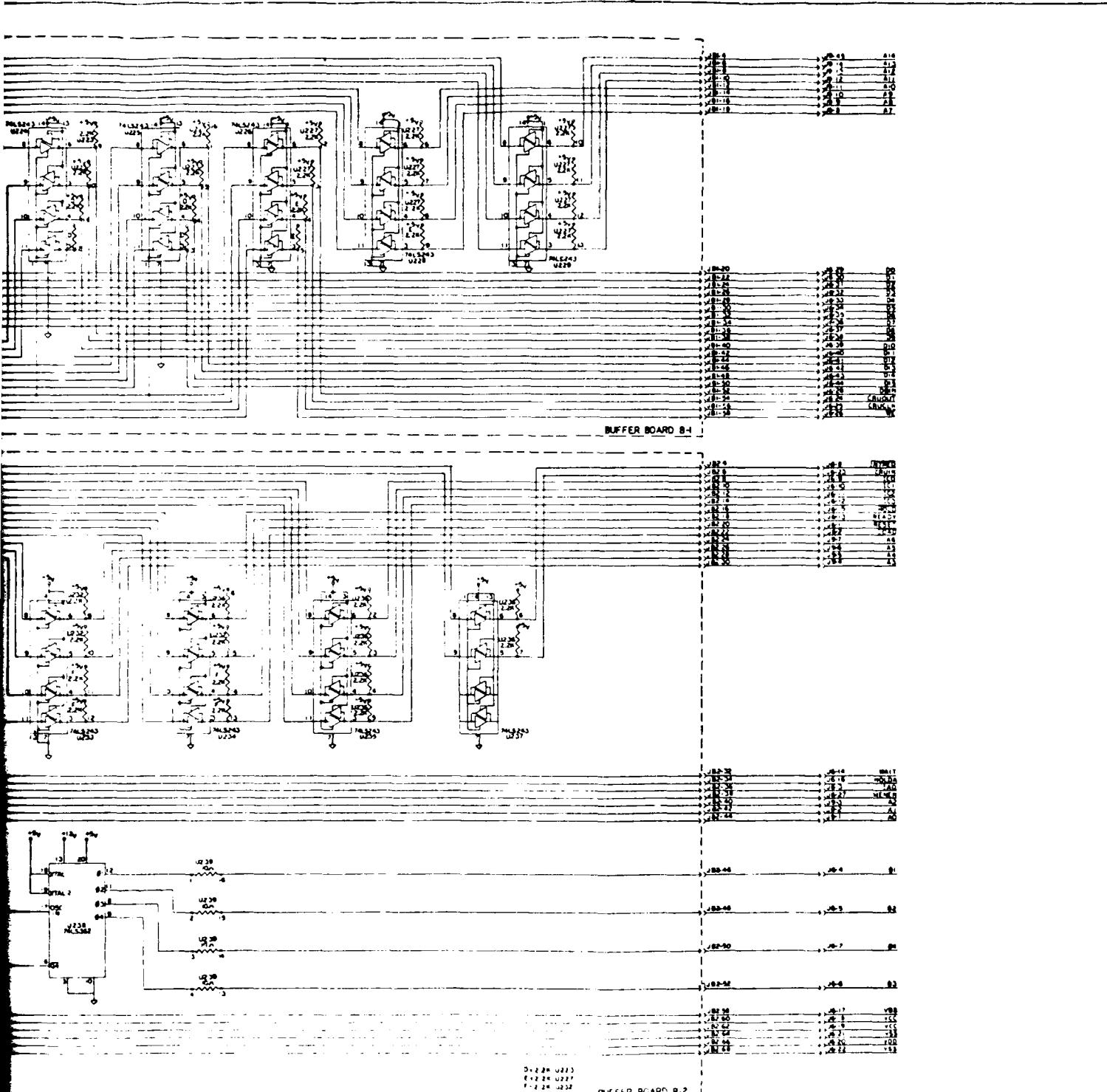
BUFFER BOARD A 2

SPIRE CORPORATION  
4400  
4400-A  
4400-B  
4400-C

BUFFER BOARDS

4D656 303 0222





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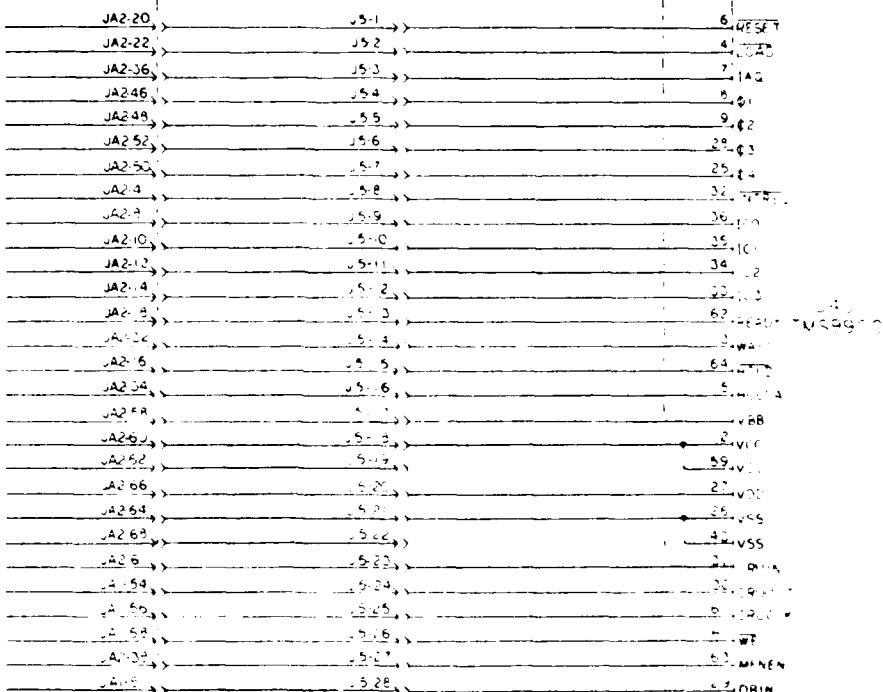
## NOTES

D

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B

A



BUFFER SCALAR A-18A-2

### WCC, PRIDE, AND EGO

REVISIONS			
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5.42	← J5.30	← JA1.22
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6.4	← J7.21	← JA1.4

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209	INCHES		MM	CM		
210	INCHES		MM	CM		
211	INCHES		MM	CM		
212	INCHES		MM	CM		
213	INCHES		MM	CM		
214	INCHES		MM	CM		
215	INCHES		MM	CM		
216	INCHES		MM	CM		
217	INCHES		MM	CM		
218	INCHES		MM	CM		
219	INCHES		MM	CM		
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221	INCHES		MM	CM		
222	INCHES		MM	CM		
223	INCHES		MM	CM		
224	INCHES		MM	CM		
225	INCHES		MM	CM		
226	INCHES		MM	CM		
227	INCHES		MM	CM		
228	INCHES		MM	CM		
229	INCHES		MM	CM		
230	INCHES		MM	CM		
231	INCHES		MM	CM		
232	INCHES		MM	CM		
233	INCHES		MM	CM		
234	INCHES		MM	CM		
235	INCHES		MM	CM		
236	INCHES		MM	CM		
237	INCHES		MM	CM		
238	INCHES		MM	CM		
239	INCHES		MM	CM		
240	INCHES		MM	CM		
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242	INCHES		MM	CM		
243	INCHES		MM	CM		
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250	INCHES		MM	CM		
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253	INCHES		MM	CM		
254	INCHES		MM	CM		
255	INCHES		MM	CM		
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258	INCHES		MM	CM		
259	INCHES		MM	CM		
260	INCHES		MM	CM		
261	INCHES		MM	CM		
262	INCHES		MM	CM		
263	INCHES		MM	CM		
264	INCHES		MM	CM		
265	INCHES		MM	CM		
266	INCHES		MM	CM		
267	INCHES		MM	CM		
268	INCHES		MM	CM		
269	INCHES		MM	CM		
270	INCHES		MM	CM		
271	INCHES		MM	CM		
272	INCHES		MM	CM		
273	INCHES		MM	CM		
274	INCHES		MM	CM		
275	INCHES		MM	CM		
276	INCHES		MM	CM		
277	INCHES		MM	CM		
278	INCHES		MM	CM		
279	INCHES		MM	CM		
280	INCHES		MM	CM		

the *Journal of the American Medical Association* (JAMA) and the *Journal of the American Dental Association* (JADA) have been merged into a single journal, *Journal of the American Medical and Dental Associations* (JAMDA).

## NOTES

D

C

B

A

JB2.31	6.3	4.5
JB2.32	6.4	4.6
JB2.33	6.3	4.7
JB2.34	6.4	4.8
JB2.35	6.4	4.9
JB2.36	6.5	5.0
JB2.37	6.5	5.1
JB2.38	6.5	5.2
JB2.39	6.5	5.3
JB2.40	6.5	5.4
JB2.41	6.5	5.5
JB2.42	6.5	5.6
JB2.43	6.5	5.7
JB2.44	6.5	5.8
JB2.45	6.5	5.9
JB2.46	6.5	6.0
JB2.47	6.5	6.1
JB2.48	6.5	6.2
JB2.49	6.5	6.3
JB2.50	6.5	6.4
JB2.51	6.5	6.5
JB2.52	6.5	6.6
JB2.53	6.5	6.7
JB2.54	6.5	6.8
JB2.55	6.5	6.9
JB2.56	6.5	7.0
JB2.57	6.5	7.1
JB2.58	6.5	7.2
JB2.59	6.5	7.3
JB2.60	6.5	7.4
JB2.61	6.5	7.5
JB2.62	6.5	7.6
JB2.63	6.5	7.7
JB2.64	6.5	7.8
JB2.65	6.5	7.9
JB2.66	6.5	8.0
JB2.67	6.5	8.1
JB2.68	6.5	8.2
JB2.69	6.5	8.3
JB2.70	6.5	8.4
JB2.71	6.5	8.5
JB2.72	6.5	8.6
JB2.73	6.5	8.7
JB2.74	6.5	8.8
JB2.75	6.5	8.9
JB2.76	6.5	9.0
JB2.77	6.5	9.1
JB2.78	6.5	9.2
JB2.79	6.5	9.3
JB2.80	6.5	9.4
JB2.81	6.5	9.5
JB2.82	6.5	9.6
JB2.83	6.5	9.7
JB2.84	6.5	9.8
JB2.85	6.5	9.9
JB2.86	6.5	10.0
JB2.87	6.5	10.1
JB2.88	6.5	10.2
JB2.89	6.5	10.3
JB2.90	6.5	10.4
JB2.91	6.5	10.5
JB2.92	6.5	10.6
JB2.93	6.5	10.7
JB2.94	6.5	10.8
JB2.95	6.5	10.9
JB2.96	6.5	11.0
JB2.97	6.5	11.1
JB2.98	6.5	11.2
JB2.99	6.5	11.3
JB2.100	6.5	11.4

BUFFER BOARDS B-3B-2

MCAC PROCES

REVISIONS  
ZONE LTR.      DESCRIPTION      DATE      APPROVED

1	.6.29	.28.25
2	.6.32	.28.22
3	.6.31	.28.24
4	.6.32	.28.26
5	.6.33	.28.28
6	.6.34	.28.30
7	.6.35	.28.32
8	.6.36	.28.34
9	.6.37	.28.36
10	.6.38	.28.38
11	.6.39	.28.40
12	.6.40	.28.42
13	.6.41	.28.44
14	.6.42	.28.46
15	.6.43	.28.48
16	.6.44	.28.50
17	.9.1	.28.44
18	.9.2	.28.42
19	.9.3	.28.40
20	.9.4	.28.38
21	.9.5	.28.28
22	.9.6	.28.26
23	.9.7	.28.24
24	.9.8	.28.22
25	.9.9	.28.16
26	.9.10	.28.14
27	.9.11	.28.12
28	.9.12	.28.10
29	.9.13	.28.08
30	.9.14	.28.06
31	.9.15	.28.04

BUFFER BOARDS B-1 & B-2

ITEM	REV	REQ	CODE	PART NO. OR IDENTIFYING NO.	DESCRIPTION	MATERIAL	SPEC
PARTS LIST							
<small>DIMENSIONS ARE IN INCHES. DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS. UNLESS OTHERWISE SPECIFIED TOLERANCES ARE</small>				CONTR NO	<small>SPIRE CORPORATION BEDFORD MASS 01730</small>		
<small>1/8" MACH.      INCHES      MM</small>				DR 1 2 3 4 5 1/2 25/32	<small>spire</small>		
<small>2 PLATES</small>				APPO	<small>PROCESSOR</small>		
<small>1 PLATE</small>				APPO	<small>SIZE      CONFIDENTIAL      DRAWING NO</small>		
<small>FRACTIONS</small>				<small>4D656      7-0205</small>			
NEXT ASSY	USED ON	MATERIAL		DRAWING APPL			
APPLICATION				DRAWING APPL			
				SCALE	SHEET 27		

## NOTES

D

C

B

A

U16

RESET	5	4	AV 9428
LOAD	4	2	AV 9428
IC1	2	3	AV 9428
IC2	9	4	AV 9428
IC3	5	5	AV 9428
IC4	2	6	AV 9428
IC5	6	7	AV 9428
IC6	3	8	AV 9428
IC7	36	9	AV 9428
IC8	35	10	AV 9428
IC9	34	11	AV 9428
IC10	33	12	AV 9428
READY	62	13	AV 9428
WA	63	14	AV 9428
WXA	64	15	AV 9428
WXLCA	5	16	AV 9428
Y88	2	17	AV 9428
YCC	59	18	AV 9428
YCL	58	19	AV 9428
VOO	26	20	AV 9428
VSS	26	21	AV 9428
Y2	5	22	AV 9428
CP	2	23	AV 9428
CP	2	24	AV 9428
WE	6	25	AV 9428
WB1N	53	26	AV 9428
WB2N	2	27	AV 9428
WB3	1	28	AV 9428
WB4	42	29	AV 9428
WB5	43	30	AV 9428
WB6	14	31	AV 9428
WB7	15	32	AV 9428
WB8	16	33	AV 9428
WB9	49	34	AV 9428
WB10	5	35	AV 9428
WB11	51	36	AV 9428
WB12	52	37	AV 9428
WB13	53	38	AV 9428
WB14	54	39	AV 9428
WB15	55	40	AV 9428
WB16	56	41	AV 9428
WB17	57	42	AV 9428
WB18	58	43	AV 9428
WB19	59	44	AV 9428
WB20	60	45	AV 9428
WB21	61	46	AV 9428
WB22	62	47	AV 9428
WB23	63	48	AV 9428
WB24	64	49	AV 9428
WB25	65	50	AV 9428
WB26	66	51	AV 9428
WB27	67	52	AV 9428
WB28	68	53	AV 9428
WB29	69	54	AV 9428
WB30	70	55	AV 9428
WB31	71	56	AV 9428
WB32	72	57	AV 9428
WB33	73	58	AV 9428
WB34	74	59	AV 9428
WB35	75	60	AV 9428
WB36	76	61	AV 9428
WB37	77	62	AV 9428
WB38	78	63	AV 9428
WB39	79	64	AV 9428
WB40	80	65	AV 9428
WB41	81	66	AV 9428
WB42	82	67	AV 9428
WB43	83	68	AV 9428
WB44	84	69	AV 9428
WB45	85	70	AV 9428
WB46	86	71	AV 9428
WB47	87	72	AV 9428
WB48	88	73	AV 9428
WB49	89	74	AV 9428
WB50	90	75	AV 9428
WB51	91	76	AV 9428
WB52	92	77	AV 9428
WB53	93	78	AV 9428
WB54	94	79	AV 9428
WB55	95	80	AV 9428
WB56	96	81	AV 9428
WB57	97	82	AV 9428
WB58	98	83	AV 9428
WB59	99	84	AV 9428
WB60	100	85	AV 9428
WB61	101	86	AV 9428
WB62	102	87	AV 9428
WB63	103	88	AV 9428
WB64	104	89	AV 9428
WB65	105	90	AV 9428
WB66	106	91	AV 9428
WB67	107	92	AV 9428
WB68	108	93	AV 9428
WB69	109	94	AV 9428
WB70	110	95	AV 9428
WB71	111	96	AV 9428
WB72	112	97	AV 9428
WB73	113	98	AV 9428
WB74	114	99	AV 9428
WB75	115	100	AV 9428
WB76	116	101	AV 9428
WB77	117	102	AV 9428
WB78	118	103	AV 9428
WB79	119	104	AV 9428
WB80	120	105	AV 9428
WB81	121	106	AV 9428
WB82	122	107	AV 9428
WB83	123	108	AV 9428
WB84	124	109	AV 9428
WB85	125	110	AV 9428
WB86	126	111	AV 9428
WB87	127	112	AV 9428
WB88	128	113	AV 9428
WB89	129	114	AV 9428
WB90	130	115	AV 9428
WB91	131	116	AV 9428
WB92	132	117	AV 9428
WB93	133	118	AV 9428
WB94	134	119	AV 9428
WB95	135	120	AV 9428
WB96	136	121	AV 9428
WB97	137	122	AV 9428
WB98	138	123	AV 9428
WB99	139	124	AV 9428
WB100	140	125	AV 9428
WB101	141	126	AV 9428
WB102	142	127	AV 9428
WB103	143	128	AV 9428
WB104	144	129	AV 9428
WB105	145	130	AV 9428
WB106	146	131	AV 9428
WB107	147	132	AV 9428
WB108	148	133	AV 9428
WB109	149	134	AV 9428
WB110	150	135	AV 9428
WB111	151	136	AV 9428
WB112	152	137	AV 9428
WB113	153	138	AV 9428
WB114	154	139	AV 9428
WB115	155	140	AV 9428
WB116	156	141	AV 9428
WB117	157	142	AV 9428
WB118	158	143	AV 9428
WB119	159	144	AV 9428
WB120	160	145	AV 9428
WB121	161	146	AV 9428
WB122	162	147	AV 9428
WB123	163	148	AV 9428
WB124	164	149	AV 9428
WB125	165	150	AV 9428
WB126	166	151	AV 9428
WB127	167	152	AV 9428
WB128	168	153	AV 9428
WB129	169	154	AV 9428
WB130	170	155	AV 9428
WB131	171	156	AV 9428
WB132	172	157	AV 9428
WB133	173	158	AV 9428
WB134	174	159	AV 9428
WB135	175	160	AV 9428
WB136	176	161	AV 9428
WB137	177	162	AV 9428
WB138	178	163	AV 9428
WB139	179	164	AV 9428
WB140	180	165	AV 9428
WB141	181	166	AV 9428
WB142	182	167	AV 9428
WB143	183	168	AV 9428
WB144	184	169	AV 9428
WB145	185	170	AV 9428
WB146	186	171	AV 9428
WB147	187	172	AV 9428
WB148	188	173	AV 9428
WB149	189	174	AV 9428
WB150	190	175	AV 9428
WB151	191	176	AV 9428
WB152	192	177	AV 9428
WB153	193	178	AV 9428
WB154	194	179	AV 9428
WB155	195	180	AV 9428
WB156	196	181	AV 9428
WB157	197	182	AV 9428
WB158	198	183	AV 9428
WB159	199	184	AV 9428
WB160	200	185	AV 9428
WB161	201	186	AV 9428
WB162	202	187	AV 9428
WB163	203	188	AV 9428
WB164	204	189	AV 9428
WB165	205	190	AV 9428
WB166	206	191	AV 9428
WB167	207	192	AV 9428
WB168	208	193	AV 9428
WB169	209	194	AV 9428
WB170	210	195	AV 9428
WB171	211	196	AV 9428
WB172	212	197	AV 9428
WB173	213	198	AV 9428
WB174	214	199	AV 9428
WB175	215	200	AV 9428
WB176	216	201	AV 9428
WB177	217	202	AV 9428
WB178	218	203	AV 9428
WB179	219	204	AV 9428
WB180	220	205	AV 9428
WB181	221	206	AV 9428
WB182	222	207	AV 9428
WB183	223	208	AV 9428
WB184	224	209	AV 9428
WB185	225	210	AV 9428
WB186	226	211	AV 9428
WB187	227	212	AV 9428
WB188	228	213	AV 9428
WB189	229	214	AV 9428
WB190	230	215	AV 9428
WB191	231	216	AV 9428
WB192	232	217	AV 9428
WB193	233	218	AV 9428
WB194	234	219	AV 9428
WB195	235	220	AV 9428
WB196	236	221	AV 9428
WB197	237	222	AV 9428
WB198	238	223	AV 9428
WB199	239	224	AV 9428
WB200	240	225	AV 9428
WB201	241	226	AV 9428
WB202	242	227	AV 9428
WB203	243	228	AV 9428
WB204	244	229	AV 9428
WB205	245	230	AV 9428
WB206	246	231	AV 9428
WB207	247	232	AV 9428
WB208	248	233	AV 9428
WB209	249	234	AV 9428
WB210	250	235	AV 9428
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WB212	252	237	AV 9428
WB213	253	238	AV 9428
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WB216	256	241	AV 9428
WB217	257	242	AV 9428
WB218	258	243	AV 9428
WB219	259	244	AV 9428
WB220	260	245	AV 9428
WB221	261	246	AV 9428
WB222	262	247	AV 9428
WB223	263	248	AV 9428
WB224	264	249	AV 9428
WB225	265	250	AV 9428
WB226	266	251	AV 9428
WB227	267	252	AV 9428
WB228	268	253	AV 9428
WB229	269	254	AV 9428
WB230	270	255	AV 9428
WB231	271	256	AV 9428
WB232	272	257	AV 9428
WB233	273	258	AV 9428
WB234	274	259	AV 9428
WB235	275	260	AV 9428
WB236	276	261	AV 9428
WB237	277	262	AV 9428
WB238	278	263	AV 9428
WB239	279	264	AV 9428
WB240	280	265	AV 9428
WB241	281	266	AV 9428
WB242	282	267	AV 9428
WB243	283	268	AV 9428
WB244	284	269	AV 9428
WB245	285	270	AV 9428
WB246	286	271	AV 9428
WB247	287	272	AV 9428
WB248	288	273	AV 9428
WB249	289	274	AV 9428
WB250	290	275	AV 9428
WB251	291	276	AV 9428
WB252	292	277	AV 9428
WB253	293	278	AV 9428
WB254	294	279	AV 9428
WB255	295	280	AV 9428



APPENDIX II  
ASSEMBLY LANGUAGE CODES FOR THE  
990/100M CONTROL OF THE TEST SYSTEM

0110		101	111000	
0115	2400	1010	2400	START ADDRESS OF CODE TO RUN AT C000
0120	7723	114P	7723	OPEN MORE SPACES
0130	7743	114P	7743	CLOSE MORE SPACES
0140	7761	114P	7761	END WORKSPACE
0150	7763	124P	7763	END WORKSPACE
0160	0460	2PA	0460	MACHINE CODE FOR SP
0170	0016	INT5	0016	INTERRUPT 5 VECTOR
0180	0012	INT4	0012	INTERRUPT 4 VECTOR
0190	7724	VECT	7724	VMIC VECTOR
01A0	0004	BIT	0004	NUMBER OF BYTES PER ERROR
01B0	0004	BUU	0004	NUMBER OF ERRORS ALLOWED IN ITBS
01C0	4600	F	4600	ASCII F
01D0	5200	2	5200	ASCII 2
01E0	1300	6110	1300	ASCII 6
01F0	0120	CONT	0120	CONTROL BASE ADDRESS
0200	0130	INPT	0130	INPUT BASE ADDRESS
0210	0140	INTP	0140	INTERRUPT BASE ADDRESS
0220	0030	DEP	0030	DEPIAL BASE ADDRESS
0231	0009	20	0009	0
0232	0001	21	0001	1
0233	0002	22	0002	2
0234	0003	23	0003	3
0235	0004	24	0004	4
0236	0005	25	0005	5
0237	0006	26	0006	6
0238	0007	27	0007	7
0239	0008	28	0008	8
023A	0009	29	0009	9
023B	000A	210	000A	10
023C	000B	211	000B	11
023D	000C	212	000C	12
023E	000D	213	000D	13
023F	000E	214	000E	14
0240	000F	215	000F	15
0241			5 01P	INT 14
0242			5 02P	INT 11
0250	0003	*		

0230 0000	•		
0240 0000	•		
0250 E000		ADRG >E000	<<<< SETUP SEGMENT >>>>
0260 E000	•		
0270 E000 0300	SETP	LIMI 0	TURN OFF ALL INTERRUPTS
E002 0000			
0280 E004 02E0		LMPI STWP	SETUP THE WORKSPACE
E005 FF48			
0290 E003 0205		LI R5,SYNC	SYNC ENTRY POINT
E100			
0300 E003 0206		LI R6,SYMP	ADDRESS OF SYNC WORKSPACE
E002 FF28			
0310 E010 0207		LI R7,VECT	SYNC VECTOR (NP,PC)
E012 FF24			
0320 E014 0226		MOV R6,•R7+	SYNC WORKSPACE INTO SYNC VECTOR
0330 E015 0505		MOV R5,•R7	SYNC ENTRY POINT INTO SYNC VECTOR
0340 E013 0201		LI R1,BRA	MACHINE CODE FOR B6>
E014 0460			
0350 E016 0202		LI R2,E20	ESCAPE ENTRY POINT
E200			
0360 E020 0203		LI R3,E2R	ERROR ENTRY POINT
E202 E200			
0370 E024 0120		MOV DIINT5,R4	INTERRUPT 5 VECTOR PC INTO R4
E025 0016			
0380 E028 CD01		MOV R1,•R4+	B6> INTO FIRST INSTRUCTION WORD
0390 E029 C502		MOV R3,•R4	ERR ENTRY INTO SECOND WORD
1400 E021 0120		MOV DIINT4,R4	INTERRUPT 4 VECTOR PC INTO R4
E022 0012			
0410 E030 CD01		MOV R1,•R4+	FIRST INSTRUCTION WORD
0420 E032 C502		MOV R2,•R4	E20 ENTRY INTO SECOND WORD
0430 E034 0546		DECT R6	
0440 E036 0546		DECT R6	R6 NOW HAS PROPER OVERRUN ADDRESS

0450	E033	PFR0	TOP	OUT	PORLF	
	E03A	E350				
0460	E03C	2FA0		OUT	PFR	OUTPUT INITIAL QUERRY
	E03E	E354				
0470	E040	2EC0		ECHO	R0	GET RESPONSE WITH ECHO
0480	E042	PFR0		OUT	PORLF	
	E044	E350				
0490	E046	0330		CI	R0,F	IS ANSWER AN F?
	E048	4600				
0500	E04A	1304		JEO	FRES	YES. THEN JUMP TO FRES
0510	E04C	0230		CI	R0,R	IS ANSWER AN R?
	E04E	5200				
0520	E050	1314		JEO	REST	YES. THEN JUMP TO REST
0530	E052	10F2		JMP	TOP	IF NEITHER, THEN MISTAKE. TRY AGAIN
0540	E054	0203	FRES	LI	R8,ERWP	ERROR WORKSPACE POINTER INTO R8
	E056	FF68				
0550	E058	0606		MOV	R6,♦R8	OVERRUN ADDRESS INTO R6 OF ERR
0560	E05A	0201		LI	R1,BYT	NUMBER OF STORE BYTES PER ERROR
	E05C	0004				
0570	E05E	0801		MOV	R1,94(8)	PUT INTO R2 OF ERR
	E05E	0004				
0580	E062	0531		INC	R1	ROUND UP BYTES TO WORDS
0590	E064	0811		SLA	R1,1	
0600	E066	0811		SLA	R1,1	
0610	E068	0202		LI	R2,NUM	NUMBER OF ERRORS ALLOWED IN STACK
	E06A	0008				
0620	E06C	3381		MPY	R1,R2	NUMBER OF BYTES ALLOWED IN STACK 1
0630	E06E	0036		MOV	R6,R2	OVERRUN ADDRESS INTO R2
0640	E070	6033		S	R3,R2	START OF STACK INTO R2
0650	E072	0802		MOV	R2,92(8)	START OF STACK INTO R1 OF ERR
	E074	0002				
0660	E076	0802		MOV	R2,920(8)	START OF STACK INTO R10 OF ERR
0670	E078	0420	PEST	BLWP	WVECT	SYNCHRONIZE MICRO3
	E07C	FF24				
0680	E07E	0230		CI	R0,F	IS THIS A FRECHSTART?
	E080	4600				
0690	E082	1602		JME	PSU	NO. THEN RETURN AS FROM ESC
0700	E084	0460		B	CODE	FREST START. SO GO TO CODE
	E086	E800				
0710	E088	0220	PSU	LWPI	ECWP	ESC WORKSPACE
	E08A	FF3C				
0720	E08C	0330		RTWP		
0730	E08E	♦				

0740 E03E	•		
0750 E03E	•		
0760 E100		ADRS 1E100	LOCK CYCLO SEGMENT
0770 E100	•		
0780 E100 0200	SWTC	LI R12,CONT	BASE ADDRESS FOR CONTROL
	E102 0120		
0790 E104 1E00	DBZ 0		TRIGGER THE RESET
0800 E105 10FF	WAIT	JMP	WAIT HERE FOR THE RESET
0810 E108 02E0	REEN	LWPI SWMP	RELOAD WORKSPACE POINTER UPON REEN
	E108 FF23		
0820 E10C 0200		LI R12,SER	BASE ADDRESS FOR R12 OUTPUT
	E10E 0030		
0830 E110 1D12	DBZ 10		ENABLE RECEIVER INTERRUPT
0840 E112 0200		LI R12,CONT	BASE ADDRESS FOR CONTROL
	E114 0120		
0850 E116 1D03	DBZ 3		QUIESCENT CLK
0860 E118 1D02	DBZ 2		QUIESCENT SET
0870 E11A 1E04	DBZ 4		RESET SYSTEM
0880 E11C 1D04	DBZ 4		
0890 E11E 1E01	DBZ 1		TURN ON SYSTEM
0900 E120 0200		LI R12,INRR	INTERRUPT BASE ADDRESS
	E122 0100		
0910 E124 1D04	DBZ 4		ENABLE ESC AT 9901
0920 E126 1D05	DBZ 5		ENABLE ERR AT 9901
0930 E128 0380	PTWP		
0940 E12A	•		
0950 E12A	•		
0960 E12A	•		
0970 E200		ADRS 1E200	LOCK ESCAPE SEGMENT
0980 E200	•		
0990 E200 0300	EIC	LIMI 0	TURN OFF ALL INTERRUPTS
	E202 0000		
1000 E204 0200		LI R12,CONT	BASE ADDRESS FOR CONTROL
	E206 0120		
1010 E208 1D01	DBZ 1		TURN OFF SYSTEM
1020 E20A 0400	CLR 20		PREPARE R0
1030 E20C 0200		LI R12,SER	SERIAL BASE ADDRESS
	E20E 0030		
1040 E210 3600	STCR R0,8		SET INTERRUPT CHARACTER
1050 E212 1D12	DBZ 10		CLEAR INTERRUPT
1060 E214 0230	SI R0,6000		IS IT AN ESC?
	E216 1200		
1070 E218 1D01	JED MON		YES, THEN JUMP TO MON
1080 E21A 0380	PTWP		NO, THEN RETURN
1090 E21C 0580	MON	BL 0-80	GO TO MONITOR
	E21E 0480		
1100 E220	•		

1110 E220	►			
1120 E220	►			
1130 E250		ADRS6 → E250		CODE ERROR SEGMENT ↗
1140 E250	►			
1150 E250 0200 EPR		LI R12+CONT		CONTROL BASE ADDRESS
E252 0120				
1170 E254 1201		SP0 1		TURN OFF SYSTEM
1180 E256 0022		MOV R2+R3		MAX BYTE COUNT INTO R3
1190 E258 0248		MOV R14+R1+		STORE PC AT ERROR ON STACK
1200 E258 0648		DEC R3		DECREMENT THE BYTE COUNT
1210 E250 1202		DB2 2		SETUP THE READ
1220 E252 1D02		DB0 2		
1230 E250 0200 READ		LI R12+INPT		INPUT BASE ADDRESS
E252 0130				
1240 E264 3611		STOR *R1+3		READ ONE BYTE ONTO STACK
1250 E266 0531		INC R1		INCREMENT ERROR STACK POINTER
1260 E268 0503		DEC R3		DECREMENT BYTE COUNT
1270 E264 1205		JEP DONE		GO TO DONE IF FINISHED
1280 E250 0200		LI R12+CONT		CONTROL BASE ADDRESS
E252 0120				
1290 E270 1203		DB2 3		MOVE TO NEXT BYTE
1300 E272 1203		DB0 3		
1310 E274 1075		JMP READ		GO GET NEXT BYTE
1320 E276 0531 DONE		INC R1		ROUND UP ERROR STACK POINTER
1330 E278 0811		CPA R1+1		
1340 E278 0811		CLA R1+1		
1350 E270 0022		MOV R2,R3		BYTE COUNT
1360 E272 0533		INC R3		ROUND IT UP
1370 E270 0810		CPA R3+1		
1380 E272 0418		CLA R3+1		
1390 E284 8001		R R1,R3		WILL WE OVERRUN ON NEXT ERROR?
1400 E226 8003		C R3,R0		
1410 E228 1B03		JH OVER		IF YES JUMP TO OVER
1420 E228 0420		BUMP BVECT		SYNCHRONIZE MICROS
E220 FF24				
1430 E228 0380		RTUP		CONTINUE WHERE WE LEFT OFF
1440 E220 2FA0 OVER		OUT \$H0D0		OUTPUT OVERRUN MESSAGE
E222 E278				
1450 E224 0204		LI R4+ECWP		ESCAPE WORKSPACE POINTER TO R4
E226 FF80				
1460 E228 0900		MOV R13+R26(4)		SETUP PSEUDO ESC RETURN
E224 0014				
1470 E228 0908		MOV R14+R28(4)		
E226 0016				
1480 E220 090F		MOV R15+R30(4)		
E222 0018				
1490 E224 004A		MOV R10+R1		RESTORE START OF STACK TO R1
1500 E226 0580		BL R+R0		BRANCH TO MONITOR
E228 0030				
1510 E22A	►			

1520 E284 •  
1530 E284 •  
1540 E350 • ADIG >E350 <<< MESSAGE LIST >>>  
1550 E230 •  
15 0 E350 0004 CRLF DATA >000A+0  
E352 0000  
1570 E354 4552 FR TEXT 'REFRESH START OR RESTART? (F OR R)'  
E356 4553  
E358 4320  
E360 5354  
E360 4152  
E362 5420  
E360 4752  
E362 2052  
E364 4553  
E366 5441  
E368 5254  
E368 3820  
E360 3846  
E362 2048  
E370 5220  
E372 5229  
1580 E374 0003 DATA >000A+0  
E376 0000  
1590 E378 4E4F N0M0 TEXT 'NO MORE ROOM IN ERROR STACK.'  
E378 2040  
E370 4F53  
E372 4520  
E380 524F  
E382 4F4D  
E384 2049  
E386 4E20  
E388 4552  
E38A 524F  
E390 5220  
E38E 5354  
E390 4143  
E392 482E  
1600 E394 000A DATA >000A+0  
E396 0000  
2000 END

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